What is claimed is:

1. A stack-type capacitor comprising:

a lower electrode;

a dielectric layer formed on the lower electrode; and

an upper electrode formed on the dielectric layer,

wherein the lower electrode includes:

a first metal layer having a cylindrical shape; and

a second metal layer filled in the first metal layer.

2. The capacitor as claimed in claim 1, wherein the first metal layer is a ruthenium layer and the second metal layer is a nitride and aluminum layer.

3. The capacitor as claimed in claim 2, wherein the nitride and aluminum layer is a titanium aluminum nitride layer or a tantalum aluminum nitride layer.

4. The capacitor as claimed in claim 2, wherein the upper electrode is a ruthenium layer.

5. A semiconductor memory device including a stack-type capacitor, the device comprising a transistor and a capacitor,

wherein the capacitor includes:

a lower electrode;

a dielectric layer formed on the lower electrode; and

an upper electrode formed on the dielectric layer,

wherein the lower electrode includes:

a first metal layer having a cylindrical shape; and

a second metal layer filled in the first metal layer.

6. The device as claimed in claim 5, wherein the transistor is electrically connected to the capacitor by a conductive plug.

7. The device as claimed in claim 6, wherein a diffusion barrier layer is formed between the lower electrode and the conductive plug.

8. The device as claimed in claim 7, wherein the diffusion barrier layer is a titanium nitride layer.

9. The device as claimed in claim 5, wherein the first metal layer is a ruthenium layer, and the second metal layer is a nitride and aluminum layer.

10. The device as claimed in claim 9, wherein the nitride and aluminum layer is a titanium aluminum nitride layer or a tantalum aluminum nitride layer.

11. The device as claimed in claim 9, wherein the upper electrode is a ruthenium layer.

12. A method of manufacturing a stack-type capacitor, the method comprising:

(a) sequentially stacking an etch stop layer and an interlayer dielectric on a substrate and forming a via hole by patterning the interlayer dielectric and the etch stop layer;

(b) sequentially forming a first metal layer and a second metal layer in the via hole and on the interlayer dielectric;

(c) exposing the interlayer dielectric;

(d) forming a lower electrode formed of the first metal layer and the second metal layer by removing the interlayer dielectric; and

(e) sequentially depositing a dielectric layer and an upper electrode on the lower electrode,

wherein the first metal layer is formed by atomic layer deposition.

13. The method as claimed in claim 12, wherein the first metal layer is formed of ruthenium and the second metal layer is formed of titanium aluminum nitride or tantalum aluminum nitride.

14. The method as claimed in claim 13, wherein the upper electrode is formed of ruthenium.

15. The method as claimed in claim 12, wherein (b) includes:

absorbing a ruthenium precursor to a resultant structure of (a);

purging any remaining ruthenium precursor;

decomposing the ruthenium precursor by absorbing an oxygen gas to the absorbed ruthenium precursor layer, to thereby form a ruthenium oxide layer;

purging any remaining oxygen gas; and

reducing the ruthenium oxide layer by supplying a hydrogen gas thereto.

16. The method as claimed in claim 15, further comprising absorbing a halogen-series material to the resultant structure of (a) before absorbing the ruthenium precursor.

17. The method as claimed in claim 16, wherein the halogen-series material is iodine.

18. A method of manufacturing a semiconductor memory device including a stack-type capacitor, the method comprising:

(a) forming a transistor on a substrate;

(b) forming a first interlayer dielectric on the substrate;

(c) forming a contact hole in the first interlayer dielectric to expose a predetermined region of the transistor;

(d) forming a conductive plug in the contact hole;

(e) forming an insulating layer on the first interlayer dielectric, patterning the insulating layer until the conductive plug is exposed, and forming a diffusion barrier layer on the exposed portion;

(f) sequentially stacking an etch stop layer and a second interlayer dielectric on the first interlayer dielectric and patterning the second interlayer dielectric and the etch stop layer to expose the diffusion barrier layer;

(g) sequentially forming a first metal layer and a second metal layer on a resultant structure of (f);

(h) exposing the second interlayer dielectric;

(i) forming a lower electrode formed of the first metal layer and the second metal layer by removing the second interlayer dielectric; and

(j) sequentially depositing a dielectric layer and an upper electrode on the lower electrode,

wherein the first metal layer is formed by atomic layer deposition.

19. The method as claimed in claim 18, wherein the first metal layer is formed of ruthenium and the second metal layer is formed of titanium aluminum nitride.

20. The method as claimed in claim 19, wherein the upper electrode is formed of ruthenium.

21. The method as claimed in claim 18, wherein the diffusion barrier layer is formed of titanium nitride.

22. The method as claimed in claim 21, wherein (g) includes:

absorbing a ruthenium precursor on a resultant structure of (f);

purging any remaining ruthenium precursor;

decomposing the ruthenium precursor by absorbing an oxygen gas to the absorbed ruthenium precursor layer, to form a ruthenium oxide layer;

purging any remaining oxygen gas; and

reducing the ruthenium oxide layer by supplying a hydrogen gas thereto.

23. The method as claimed in claim 22, further comprising absorbing a halogen-series material to the resultant structure of (f) before absorbing the ruthenium precursor.

24. The method as claimed in claim 23, wherein the halogen-series material is iodine.